What is claimed is:

1. A low power audio processor comprising:

a bit stream processing unit for bit processing an applied audio stream into a bit processed audio stream and for decoding the bit processed audio stream to have a format conducive to digital signal processing;

a digital signal processing unit for digital signal processing the decoded bit processed audio stream received from the bit stream processing unit to develop a digital signal processed audio stream;

a post processing unit for receiving the digital signal processed audio stream from the digital signal processing unit to develop final audio data;

a host interface unit for interfacing with an external device to provide an audio parallel stream received from the external device to the bit stream processing unit;

a power control unit for determining a power state for each of the bit stream processing unit, the digital signal processing unit and the post processing unit in response to: (1) a request signal and an acknowledge signal between the digital signal processing unit and the post processing unit, (2) a power down signal, and (3) a source clock, the power control unit outputting a determined power state as a power mode signal; and

an internal clock signal generator unit for generating clock signals, each of the clock signals corresponding to a respective one of the bit stream processing unit, the digital signal processing unit and the post processing unit.

2. The audio processor as recited in claim 1, further comprising a memory device for temporarily storing data processed at each of the bit stream processing unit, the digital a signal processing unit and the post processing unit.

3. The audio processor as recited in claim 1, wherein the internal clock generator includes:

a first multiplexor for selectively outputting one of a DC level and the source

clock in response to the power down signal;

a divider for dividing the output of the first multiplexor by a predetermined factor; and

second, third and fourth multiplexors, for selecting respective ones of the clock signals from the divider and the DC level in response to the power state of a corresponding one of the bit stream processing unit, the digital signal processing unit and to post processing unit, each of the second, third and fourth multiplexors outputting, a selected signal to a respective one of the bit stream processing, digital signal processing and post processing units to output the selected signal to the corresponding processing unit.

4. The audio processor as recited in claim 3, wherein the internal clock generator further includes a logic device for OR operating the outputs of the second, third and fourth multiplexors to drive a memory device.